REMARKS/ARGUMENTS:

In the specification amendments have been made to pages 1, 10, 24, 26 and 27; no new matter has been added.

No amendments have been made to the drawings.

Claims 1-42 remain pending in this application. No claims have been cancelled or added. Claims 1, 3, 5, 21, 22, 24, 26 and 34 have been amended.

The Examiner is thanked for pointing out editorial errors in the specification and claims and for the detailed discussion of the references which, although applicant does not necessarily concur with the Examiner's interpretation of particular references, has been helpful in reviewing and addressing the various grounds of rejection.

Objections to the Drawings

The specification has been amended on page 27 to address the Examiner's objections and no amendment of the drawings is required.

Objections to the Specification

Amendments have been made in response to the informalities noted by the Examiner on pages 26 and 27 as well as to address editorial and grammatical inconsistencies on pages 10 and 24 noted during review of the specification. As amended, page 27 now includes references "106" and "108" in a manner consistent with Fig. 4.

The related application data on page 1 also have been updated.

Claim Objections and Rejections under 35 US 112

The informalities noted by the Examiner in claims 21 and 34 have been corrected.

Allowable Claims

The indication of allowable subject matter in claims 3, 19-21, 24 and 40-42 is noted with appreciation. Claims 3 and 24 have been rewritten in independent form to include the subject matter of claims 1 and 2 in amended claim 3, and to include the subject matter of claims 22 and 23 in amended claim 24. Accordingly, amended claims 3 and 24 are believed to be in condition for allowance together with claim 5 (now dependent on claim 3) and claim 26.(now dependent on claim 24). Claims 19-21 and 40-42 remain in dependent form and are believed to be allowable as will be discussed below.

Claim Rejections under 35 US 102

Claim 22 was rejected under 35 US 102 as anticipated by US Patent 5,748,873 (Ohguro). Although not necessarily concurring with the Examiner's interpretation of Ohguro, amended system claim 22 is not anticipated by Ohguro. Claim 22 as amended parallels amended method claim 1, the network bridge feature recited in claim 1 which was not rejected under 35 US 102 and also includes recitation directed to irrecoverable errors, further distinguishing from Ohguro.

Claim Rejections under 35 US 103

In rejecting each of claims 1, 2, 4, 6-18, 23, 31, 32, 36, and 37 under 35 US 103, the Examiner has asserted those claims are obvious based at least in part on US Patent 5,748,873 (Ohguro) in view of US Patent Publication 2002/0152418 A1 (Griffin). The grounds of rejection are respectfully traversed. The reasons for traversal also applicable to amended claim 22 and its dependent claims 25, 27-30, 33-35, 38, and 39.

In establishing a prima facie case of obviousness, the claim under rejection must be considered as a whole, and each reference relied on to support the rejection must be considered in its entirety. (MPEP 2141.02) In addition, a proposed combination of references must have been suggested by the prior art and cannot change the principle of operation of the subject matter of a reference being modified. (MPEP 2143.01) The modification of Ohguro by Griffin as proposed in the Office Action fails to meet these criteria and thus a prima facie case of obviousness has not been established.

The rejection of independent claim 1, as obvious over Ohguro in view of Griffin relies on disclosure by the primary reference (Ohguro) of a method of error recovery in a lockstep computer processing system comprising a master processor and a checker processor in a computer system that ". . . causes the master processor to perform the same operation and compares the output results of the processors with each other for the purpose of detecting any fault that might exist." (Col. 1, lines 12-18). Ohguro's system is stated to have capability to "continue a process in a duplex mode if an internal fault occurs in a processor . . ." (col. 2, lines 55-57), an internal fault being one "resulting mainly from an intermittent fault and a mismatch between the processed results of both of the processors occurs" (col. 2, lines 42-46). Ohguro teaches: "One of the processors operates to write an internal state of the processor in the main memory and save it if a mismatch between the outputs of the comparing means is detected. Further means determine a factor of the fault and recognize the fault occurring in the processor based on the determined result. If it is determined that the duplicated processors can continue the process in a duplex mode, further means give a synchronous indication to the reoperating means, initialize the processors in response to a re-operating indication output when the re-operating means receives the synchronous indication, read the internal information saved in the main memory, and initiate continuation of the process." (Col. 2, line 63-col. 3, line 8; also, Abstract.) Ohguro also states "It is a third object of the present invention to provide a double processor type computer system which is capable of allowing one processor to solely continue the process if a fixed fault occurs in the other processor." An embodiment is outlined by Ohguro at col. 3, line 50 to col. 4, line 2.

Applicant concurs with the Examiner's concession that Ohguro fails to teach that his system also comprises a bridge to I/O to a network. The Examiner cites Griffin as teaching "a fault-tolerant, lockstep system comprising a bridge to a network", noting Griffin at paragraphs [0072] and [0006], and contending: *"One of ordinary skill in the art would have been motivated to substitute the network bridge of Griffin for the I/O bridge in Ohguro, because, as is explained in Griffin, paragraph [0072], said network bridge provides connection to a variety of external resources."*

The Examiner's assertion that Griffin discloses a "bridge to a network" is traversed because Griffin does no more in [0072] than teach "a connector interface (not shown) that facilitates the physical and electrical connection of the server 20 to external resources", exemplifying "an

external interface that provides a connection to an external network via, for example, an RJ-45 connector or coaxial cable connection." This does not correspond to "a bus bridge to a network" as recited in claim 1 based on Applicants' disclosure of a bus to network bridge exemplified by a PCI to Server Area Network (SAN) I/O bridge - page 9, lines 8-12. Consequently, reliance for the rejection of claim 1 on Griffin is traversed as ill founded and should be withdrawn. Amended claim 22 is also free from rejection under 35 US 103 over Ohguro in view of Griffin based on this deficiency in Griffin.

Beyond that, the Examiner's purported combination of Ohguro and Griffin fails to meet the requirements necessary to establish a prima facie case of obviousness under 35 US 103 and is therefore traversed. The Examiner has relied on Griffin by arbitrarily selecting disclosure of the connector interface disclosed in paragraph [0072], has failed to substantiate operable interchangeability as between Ohguro's I/O adapter IOA (Fig. 1) and Griffin's connector interface (e.g. RJ-45 connector or coaxial connection) as disclosed in [0072] . The Examiner also has failed to take into consideration the teaching of Griffin considered in its entirety as required by MPEP 2141.02. Considering Griffin in its entirety, it is noted that Griffin includes disclosure of operation of two computing elements to execute instructions in a fault-tolerant computer system in which ". . .the CPU boards 22 are redundant CPU boards 22 executing substantially identical instruction streams. By executing substantially identical instruction streams, the CPU boards 22 are configured in a "failover" mode. That is, at any instant in time, one CPU board 22, e.g., the second CPU board 22', remains ready to replace the first CPU board 22 upon a failure of the first CPU board 22. As a consequence of the replacement, the second CPU board 22' experiences no loss of data, as the second CPU board 22' operates in place of the first CPU board 22. . . . Similarly, the I/O subsystems 26 are redundant components configured in failover mode." (Paragraphs [0029] and [0030].) In response to detection of a difference between data output streams from two CPU boards, a "STOP" command is issued to both CPU boards ([0047]). Fault diagnosis is employed to determine which CPU board is malfunctioning, the malfunctioning CPU board is isolated and operation of the computer system continues with the other CPU board ([[0049] to [0053]).

As discussed above, the mode of operation taught by Ohguro requires that in response to detection of e.g. an intermittent fault, corrective action results in continuation of operation of both processors in a duplex mode. In contrast, Griffin teaches that in response to any fault

detection, both computers receive a STOP command and system operation is continued using only one of the computers, i.e. a simplex mode. This is contrary to the teaching of Ohguro. Modification of Ohguro by Griffin as hypothesized by the Examiner would not permit operation of Ohguro in accordance with Ohguro's teaching and would render Ohguro unsatisfactory for its intended purpose. Accordingly, the hypothesized modification of Ohguro by Griffin relied on in the Office Examiner is defective in failing meet the requirements set forth in MPEP 2143 and cannot render obvious the invention as recited in claim 1 which, *inter alia,* calls for:

> "determining if the error is a recoverable error; if the error is a recoverable error, then saving the state of either the primary or the secondary processor to a memory; disabling the bus bridge to the network; and resetting and restarting the primary and secondary processors using the saved state;"

Amended claim 1 also includes subject matter recited in claim 5 (now dependent from claim 3):

> ". . .if the error is determined to be a non-recoverable error, then disabling the bus bridge to the network before data corruption resulting from the error can propagate onto the network.

The Examiner has not shown how Griffin's connector interface (e.g. RJ-45 connector or coaxial connection) might have been disabled in the manner recited in claim 1.

Also, contrary to the Examiner's assertions in rejecting claim 5 (the same reasons used in rejecting claim 26, subject matter of which has been included in amended claim 22) this claim feature relating to irrecoverable errors is not disclosed or suggested by Ohguro or by Griffin and the ground of rejection is traversed. The Examiner contends: *"Ohguro does teach that said system comprises a bridge to I/O devices, (see col. 5, lines 63-64), and that system resources are to be reset upon detection of a recoverable error",* but does not indicate where such disclosure is made in Ohgurop. In fact, Ohguro teaches that if "an occurring fault is so light that the data copy can stay in main memory" - a recoverable error - ". . . the processor resetting program shown in FIG. 5 can be executed" (col. 9, lines 48-54) – i.e. referring to Fig. 5, CL=1 and steps C20-C50 are executed. In contrast, if the detected fault is "serious" system reset (FIG. 5, CL=0, C60) is effected as disclosed with reference to Ohguro FIG. 6 (col. 10, lines 25-55). Ohguro's system reset is different from the processor reset disclosed with reference to FIG. 5 steps C20-C50. Griffin does not remedy the deficiencies of Ohguro because, as discussed above, Griffin

teaches that in response to any fault detection, both computers receive a STOP command and system operation is continued using only one of the computers, i.e. a simplex mode; no reference to a system reset is seen in Griffin. This ground of rejection is thus inapplicable to amended claim 1 and amended claim 22.

In the rejection of claims 36 and 37 (also applicable to claims 15 and 16), the Examiner asserts: *"It is also implicit to the teachings* [of Ohguro] *that a reset of the processors includes a reset of the system comprising said processors, (note, Ohguro, col. 1, lines 66-67, and col. 2, line 1)"* Ohguro page 1, line 66 to page 2, line 5, is a continuation of col. 1, lines 59-65, and explicitly describes prior art systems (note Col. 1, line 59) regarding which Ohguro states a system reset was performed not only in response to "serious faults" but also in response to "light faults". Ohguro, in contrast to that prior art, teaches performance only of a processor reset - in response to a "light fault" and Ohguro clearly discloses that the processor resetting program disclosed with reference to Fig. 5, (CL=1 and steps C20-C50) is different from a system reset (FIG. 5, CL=0, C60 and FIG. 6 - col. 10, lines 25-55). Consequently, the Examiner's contention that Ohguro's *"reset of the processors includes a reset of the system comprising the processors"* is untenable; it contradicts Ohguro's teaching and should be withdrawn.

The rejection under 35 US 103 of claim 1, as well as the rejection of claims 11, 15, 16, 23, 31, 32, 36 and 37 should be withdrawn and those claims should be allowable. System claim 22 as amended and its dependent claims 27-30, 33-35, 38 and 39 are also not rendered unpatentable by Ohguro and Griffin for similar reasons discussed with respect to claim 1 and should be allowable.

The rejection of claims 2, 10, 12, 13, 23, 31, 33, and 34 relies in addition on US Patent 6,233,702 (Horst) but the Examiner has failed to consider Horst in its entirety as required by MPEP 2141.02 and that ground of rejection is also traversed. Horst teaches that in response to detection of divergence between two computers operating in duplex mode, operation of one of the computers is terminated leaving the other to continue operation in simplex mode – see, for example, Horst, col. 78, lines 52-59, col. 76, lines 49-53, and col. 77, lines 55-59. Consequently, Horst's teaching is inconsistent with that of Ohguro who requires that in response to detection

of e.g. an intermittent fault, corrective action results in continuation of operation of both processors in a duplex mode (col. 2, line 55 to col. 3, line 8). Modification of Ohguro by Horst, considered in its entirety, would render Ohguro unsatisfactory for its intended purpose and cannot render obvious any of claims 2, 10, 12, 13, 23, 31, 33, and 34. Moreover, the combination of Horst with Ohguro and Griffin hypothesized by the Examiner would not lead to the features recited in those claims. Claims 2, 10, 12, 13, 23, 31, 33, and 34 are believed to be allowable.

In rejecting claims 4 and 25, the Examiner also relies on US Patent 5,915,082 (Marshall) as disclosing *"a lockstep processor system in which an error, which would otherwise be determined a non-recoverable error (see col. 5, lines 28-33), is treated as a recoverable error if the secondary processor determines that it has failed, (note col. 5, lines 35-38, and col. 6, lines 62-63)."* However, the Examiner neglects to recognize that Marshal explicitly teaches in that event, "the slave processor degrades the system fault detection by simply disabling itself and disabling the lockstep feature on both processors." This is simply not the operation taught by Ohguro (e.g. see col. 3, line 55 to col. 3, line 8) nor that recited in claim 4 or claim 25. Consequently, this ground of rejection is not based on a sustainable premise and should be withdrawn and claims 4 and 25 allowed.

Claims 6-9 and 27-30 have been rejected as obvious over Ohguro (claims 27-30) or Ohguro in view of Griffin (claims 6-9) in view of US Patent 4,589,090 (Downing). The Examiner admits Ohguro fails to teach the feature recited in claims 6 and 27 but asserts: *". . . as has been shown, Ohguro does teach identifying and treating a hardware error as a recoverable error."* It is not clear where in the Office Action this disclosure by Ohguro *"has been shown"*, and the disclosure by Ohguro ". . . some (correctable internal faults) are detected inside of a processor . . . and are corrected by the hardware itself" (col. 7, lines 32-35; see also col. 3, lines 44-49) does not support the Examiner's contention. The Examiner contends: *"Downing teaches a multiprocessor system in which a hardware error that results in a loss of resource that is not being used by the primary processor is treated as a recoverable error, (see col. 6, lines 60-65)."* The Examiner also cites Downing col. 6, line 66 to col. 7, line 2 and col. 7, lines 32-42 in support of the rejection. However, this disclosure by Downing does no more than teach ". . . if it is a non-critical

hardware component, . . . machine operation can continue either unaffected or only slightly degraded" (col. 6, lines 62-65). It is not seen how this teaching would have been applicable to Ohguro and it is not treatment of a hardware error "as a recoverable error" (claims 6 and 27) as set forth in the respective parent claims 1 and 22. Regarding the Examiner's reference to Downing at col. 7, lines 32-42, it is noted Downing's teaching: "The display panel 120 informs the operator of the status of the machine and can be used to prompt the operator to take corrective action in the event of a fault in machine operation" lacks pertinence to recoverable error correction procedure recited in claim 1 or claim 22. Rejection of claims 6 and 27 has thus been shown to be untenable; withdrawal of the rejection and allowance of claims 6 and 27 is requested. With respect to claims 7-9 and 28-30, while not necessarily concurring with the Examiner's grounds of rejection, the cited disclosure of Downing does not remedy the deficiencies of Ohguro and Griffin discussed above in relation to claim 1 and those claims are believed to be allowable together with their parent claims.

With respect to claims 13 and 34, against which US Patent 6,751,749 (Hofstee) additionally has been cited; claims 14 and 35, against which US Patent 6,658,532 (Horrigan) additionally has been cited; claims 17 and 38 against which US Patent 6,327,675 (Burdett) additionally has been cited, and claims 18 and 39 against which Burdett and US Patent 5,345,583 (Davis) additionally have been cited, while not necessarily concurring with the Examiner's grounds of rejection, or that the references can properly be combined to support a rejection under 35 US 103, the cited disclosures of these supplementary references fail to remedy the deficiencies of Ohguro and Griffin discussed above in relation to claims 1 and 22 and the dependent claims listed above are believed to be allowable together with their parent claims.

CONCLUSION.

It is believed this amendment and response address all issues raised in the Office Action. Based on the claim amendments and the above discussion it is believed claims 1, 2, 4, 6-21, 22, 23, 25, and 27-39 are patentable over the cited references and in condition for allowance. Claims 3, 5, 24 and 26 should be allowable. Claims 19-21 and 40-42 still define patentable subject matter and remain.

Favorable consideration and early allowance of the pending claims are respectfully solicited. If there are any remaining issues that could be resolved by discussion, a telephone call to the undersigned attorney at (972) 862-7428 would be appreciated.

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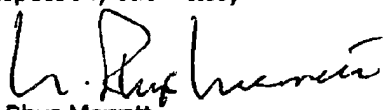
Respectfully submitted,



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